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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/697,941	10/26/2000	Lee D. Whetsel	TI-20787.2	8789

7590 04/23/2003

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EXAMINER

NGUYEN, VINH P

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 04/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/697,941	WHETSEL, LEE D.
	Examiner	Art Unit
	VINH P NGUYEN	2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 02/19/03.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 20-29 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 20-29 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413) Paper No(s). _____.
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) Notice of Informal Patent Application (PTO-152)
3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____. 6) Other: _____

1. Claims 22,24,26-27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 22, it is unclear how "d type flip flops, "And gates", "OR gates" and "delay elements" are interrelated and associated with each other.

In claim 24, it is unclear how the clock input and output buffers and a state machine are interrelated and associated with each other.

In claim 26, it is unclear how the third and fourth clock leads are interrelated and associated with clock input buffers, clock output buffers and a state machine.

In claim 27, it appears that the mode output device is improperly claimed since it is not claimed as a part of the state machine (273) as shown in figures 24E and 24G.

The dependent claims not specifically address share the same indefiniteness as they depend from rejected base claims.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 20,21,23,25 are rejected under 35 U.S.C. 102(b) as being anticipated by Khatri et al (Pat # 5,347,523).

As to claims 20, Khatri et al disclose data processing system as shown in figure 1 having a first circuit (21) having at least one mode input lead (36) for receiving a mode signal to place the first circuit in one of a first and second mode, a second circuit (16) with a mode output lead (36) connected to the mode input lead (36) and having first and second clock leads (34,32) separate from the first circuit (21), at least one of the clock leads (34,32) receiving a clock signal that controls a mode signal formed on the mode output lead (26).

As to claim 21, it appears that the first circuit (21) is a functional circuitry and the first mode is a functional mode when the lead 26 is conductive and the second mode when the lead 26 is floated.

As to claim 23, it appears that the first and second clock leads (32,34) are both capable of receiving and sending clock signals.

As to claim 25, it appears that the second circuit (16) includes more than two clock leads at clock inputs.

4. Since claims 27-29 are indefinite, no art has been applied to these instant claims.
5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Akar et al (Pat # 5,235,273) disclosse an apparatus for setting pin driver/sensor reference voltage level.

Slezak et al (Pat # 6,243,842) disclose method and apparatus for operating on a memory unit via a JTAG port.

Lee (Pat # 5,107,208) disclose a system for partitioning and testing submodule circuits of an integrated circuit.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VINH P. NGUYEN whose telephone number is (703) 305-4914.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-4900.


VINH P. NGUYEN
PRIMARY EXAMINER
ART UNIT 2829
04/17/03